AMENDMENTS TO THE CLAIMS

1. (Currently amended) A computer program product stored on a computer readable storage medium for maintaining data access during failure of a first controller in a multiple controller storage subsystem, the storage subsystem having an array of data storage devices and at least one other controller for managing the data storage, comprising computer readable program code for performing:

saving internal state information by the first controller; ~~and~~

pausing operation of the at least one other controller;

the at least one other controller saving internal state information at the time of pausing; and

continuing operation of the at least one other controller

~~method for maintaining data access during failure of a controller in a multiple controller storage subsystem, the storage subsystem having an array of data storage devices and more than one controller for managing the data storage, the method comprising:~~

~~a first controller saving internal state information; and~~

~~one or more of the other controllers carrying out the steps of:~~

~~pausing operation of the controller;~~

~~saving internal state information of the controller at the time of pausing; and~~

~~continuing operation of the controller~~.

2. (Currently amended) A computer program product ~~method~~ as claimed in claim 1, wherein the first controller detects an error in the first controller which triggers the saving of the internal state information.

3. (Currently amended) A computer program product ~~method~~ as claimed in claim 1, wherein a host computer issues a transaction to the first controller which causes ~~it~~ the first controller to save its internal state information.

4. (Currently amended) A computer program product ~~method~~ as claimed in claim 3, wherein the first controller resets after saving its internal state information.

5. (Currently amended) A computer program product ~~method~~ as claimed in claim 1, wherein the first controller instructs the at least one other controller ~~other controllers~~ to save the at least one other controller's ~~their~~ internal state information and the at least one other controller pauses operation, saves internal state information at the time of pausing, and continues operation ~~other controllers carry out the defined steps when they receive the instruction~~.

6. (Currently amended) A computer program product ~~method~~ as claimed in claim 1, wherein the at least one other controller pauses operation, saves internal state information at the time of pausing, and continues operation ~~one or more other controllers carry out the defined steps~~ when the at least one other controller detects ~~they detect~~ a loss of the first controller.

7. (Currently amended) A computer program product ~~method~~ as claimed in claim 1, wherein the first controller and the at least one other controller ~~one or more other controllers~~ save their internal state information to a storage location in each controller.

8. (Currently amended) A computer program product ~~method~~ as claimed in claim 1, wherein the first controller and the at least one other controller ~~one or more other controllers~~ save their internal state information to at least one ~~the~~ storage device ~~devices and the information is retrieved from the storage devices at a later stage~~.

9. (Currently amended) A computer program product ~~method~~ as claimed in claim 1, wherein the first controller instructs the at least one other controller ~~other controllers~~ to transfer ~~their~~ internal state information to the first controller.

10. (Currently amended) A computer program product ~~method~~ as claimed in claim 9, wherein the first controller saves the ~~combined~~ internal state information of the first controller and of the at least one other controller to the storage devices.

11. (Currently amended) A computer program product ~~method~~ as claimed in claim 1, wherein the first controller and the at least one other controller ~~multiple controllers~~ are combined on a single circuit card ~~and/or share a single memory with each controller having a separate processor~~.

12. (Currently amended) A computer program product ~~method~~ as claimed in claim 1, wherein in addition to the internal state information, at least one of the first controller and the at least one other controller save ~~a controller also saves some~~ external memory data.

13. (Currently amended) A computer program product ~~method~~ as claimed in claim 1, wherein the at least one other controller saves ~~one or more other controllers save~~ a subset of ~~their~~ internal state information.

14. (Currently amended) A computer program product ~~method~~ as claimed in claim 1, wherein the internal state information saved by the at least one other controller ~~one or more other controllers~~ is determined by an instruction received from the first controller.

15. (Currently amended) A computer program product ~~method~~ as claimed in claim 1, wherein problem analysis regarding an error in the first controller is carried out on the saved internal state information.

16. (Currently amended) A computer program product ~~method~~ as claimed in claim 1, wherein the storage subsystem comprises ~~is~~ a Fibre Channel Arbitrated Loop system and the at least one other controller comprises a ~~multiple controllers are~~ host bus adapter ~~adapters~~.

17. (Currently amended) A computer program product ~~method~~ as claimed in claim 16, wherein during the at least one other controller pausing operation, saving internal state information at the time of pausing, and continuing operation ~~defined method~~, interrupts are disabled.

18. (Currently amended) A computer program product ~~method~~ as claimed in claim 16, wherein a flag is set in a host bus adapter during the saving of internal state information to prevent overlapping saves of internal state information in that adapter.

19. (Currently amended) A computer program product ~~method~~ as claimed in claim 16, wherein the host bus adapter ~~an adapter~~ saves information relating to an interface chip.

20. (Currently amended) A method for maintaining data access during failure of a first controller in a multiple controller storage subsystem, the storage subsystem having an array of data storage devices and at least one other controller for managing the data storage, the method comprising:

the first controller saving internal state information;

pausing operation of the at least one other controller;

the at least one other controller saving internal state information at the time of pausing; and,

continuing operation of the at least one other controller

~~computer program product stored on a computer readable storage medium for maintaining data access during failure of a controller in a multiple controller storage subsystem, the storage subsystem having an array of data storage devices and more than one controller for managing the data storage, comprising computer readable program code means for performing the steps of:~~

~~a first controller saving internal state information; and~~

~~one or more of the other controllers carrying out the steps of:~~

~~pausing operation of the controller;~~

~~saving internal state information of the controller at the time of pausing; and~~

~~continuing operation of the controller~~.

Please add the following new claims:

21. (New) A computer program product as claimed in claim 8, wherein the internal state information is subsequently retrieved from the at least one storage device.

22. (New) A computer program product as claimed in claim 1, wherein the first controller and the at least one other controller share a single memory.

23. (New) An apparatus for maintaining data access during failure of a first controller in a multiple controller storage subsystem, the storage subsystem comprising at least one other controller for managing the data storage, the apparatus comprising:

the first controller comprising means for storing internal state information; and,

the at least one other controller comprising means, responsive to failure of the first controller, for pausing operation, saving internal state information at the time of pausing, and continuing operation.

24. (New) A storage subsystem comprising at least two controllers for managing data storage, the at least two controllers coupled to at least one data storage device, the storage subsystem further comprising:

a first controller of the at least two controllers adapted for saving internal state information during a failure of the first controller; and,

at least one other controller of the at least two controllers adapted for pausing operation, saving internal state information at the time of pausing, and continuing operation during the failure of the first controller.

25. (New) A storage subsystem as in claim 24, wherein an interface to at least one of the first controller and the at least one other controller comprises one of a SCSI, a Fibre Channel Arbitrated Loop and a SSA interface.

26. (New) A storage subsystem as in claim 24, wherein at least one of the first controller and the at least one other controller comprises a memory buffer.

27. (New) A storage subsystem as in claim 24, wherein the first controller and the at least one other controller share an external memory.

28. (New) A storage subsystem as in claim 24, wherein at least one of the first controller and the at least one other controller are disposed on a single circuit card.

29. (New) A storage subsystem as in claim 24, wherein each of the first controller and the at least one other controller comprise a processor.

30. (New) A storage subsystem as in claim 24, wherein the storage subsystem comprises a Fibre Channel Arbitrated Loop system and the at least one other controller comprises a host bus adapter.

31. (New) A Fibre Channel Arbitrated Loop storage system comprising:

a first set of disk drives connected to a first set of loops, and a second set of disk drives redundant with the first set of disk drives and connected to a second set of loops; wherein a first adapter is connected to the first set of loops and a second adapter is connected to the second set of loops; each adapter being adapted for issuing a command to the other adapter to save internal status data and each adapter adapted for saving internal status data and resetting.